# SSC8129GS1

## P-Channel Enhancement Mode MOSFET

### ➢ Features

| VDS | VGS | RDSON Typ. | ID |
|---|---|---|---|
| -20V | ±12V | 11mR@-4V5 | -15A |
| | | 13mR@-2V5 | |

### ➢ Description

This device is produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage power management requiring a wild range of given voltage ratings(4.5V-25V) such as load switch and battery protection.

### ➢ Applications

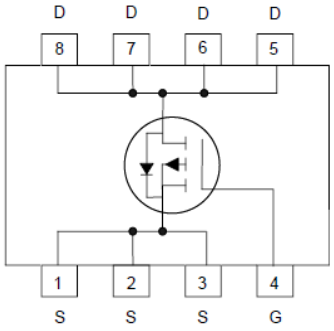
- Load Switch
- NB battery
- DCDC conversion

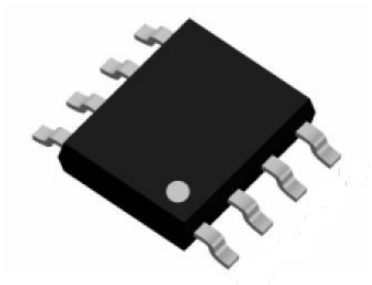
### ➢ Ordering Information

| Device | Package | Shipping |
|---|---|---|
| SSC8129GS1 | SOP8 | 2500/Reel |

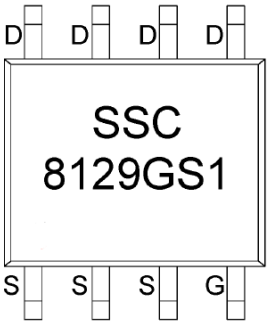
### ➢ Pin configuration

Top view



SOP8




Marking

## ➢ Absolute Maximum Ratings($T_A$=25℃ unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain-to-Source Voltage | -20 | V |
| $V_{GSS}$ | Gate-to-Source Voltage | ±12 | V |
| $I_D$ | Continuous Drain Current [a] | -15 | A |
| $I_{DM}$ | Pulsed Drain Current [b] | -41 | A |
| $P_D$ | Power Dissipation [c] | 5.5 | W |
| $P_{DSM}$ | Power Dissipation [a] | 2.5 | W |
| $T_J$ | Operation junction temperature | -55 to 150 | ℃ |
| $T_{STG}$ | Storage temperature range | -55 to 150 | ℃ |

## ➢ Thermal Resistance Ratings($T_A$=25℃ unless otherwise noted)

| Symbol | Parameter | Typical | Maximum | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-Ambient Thermal Resistance [a] | | 55 | ℃/W |
| $R_{\theta JC}$ | Junction-to-Case Thermal Resistance | | 25 | |

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 $in^2$ FR-4 board with 2oz.copper,in a still air environment with $T_A$=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

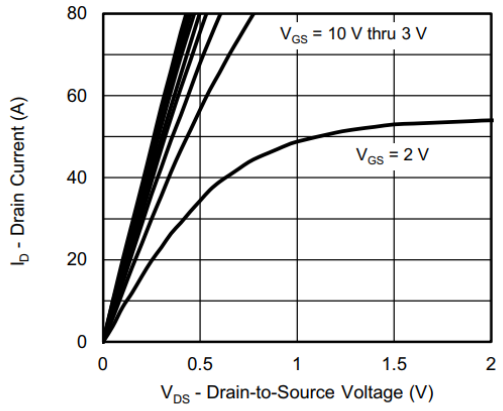
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

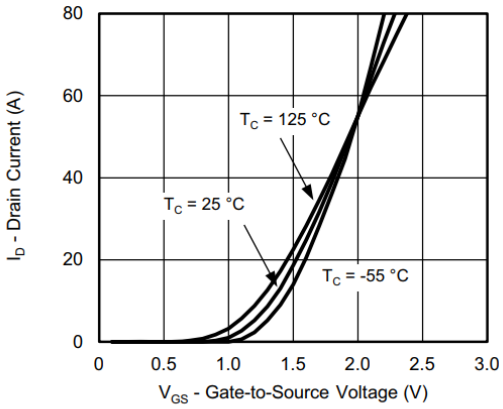
➢ **Electronics Characteristics**($T_A$=25℃ unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | VGS=0V , ID=-250uA | -20 | | | V |
| $V_{GS\ (th)}$ | Gate Threshold Voltage | VDS=VGS , ID=-250uA | -0.5 | -0.7 | -1 | V |
| $R_{DS(on)}$ | Drain-Source On-Resistance | VGS=-4.5V , ID=-10A | | 11 | 13 | mR |
| | | VGS=-2.5V , ID=-7A | | 13 | 16 | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | VDS=-16V , VGS=0V | | | -1 | uA |
| $I_{GSS}$ | Gate-Source leak current | VGS=±12V , VDS=0V | | | ±100 | nA |
| $G_{FS}$ | Trans conductance | VDS=-5V , ID=-10A | | 18 | | S |
| $V_{SD}$ | Forward Voltage | VGS=0V , IS=-2.3A | | -0.7 | -1.3 | V |
| Ciss | Input Capacitance | VDS=-15V , VGS=0V, f=1MHz | | 1820 | | pF |
| Coss | Output Capacitance | | | 489 | | |
| Crss | Reverse Transfer Capacitance | | | 663 | | |
| Qg | Total Gate charge | VGS=-4.5V , VDS=-15V, ID=-7A | | 22 | | nC |
| Qgs | Gate to Source charge | | | 2.5 | | |
| Qgd | Gate to Drain charge | | | 6 | | |
| $T_{D(ON)}$ | Turn-on delay time | VGS=-10V, VDS=-15V, RL=1.5R, RG=3R | | 11 | | ns |
| Tr | Rise time | | | 22 | | |
| $T_{D(OFF)}$ | Turn-off delay time | | | 51 | | |
| Tf | Fall time | | | 24 | | |

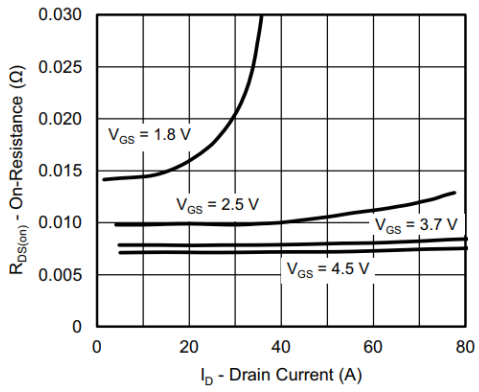
## ➢ Typical Characteristics($T_A$=25℃ unless otherwise noted)



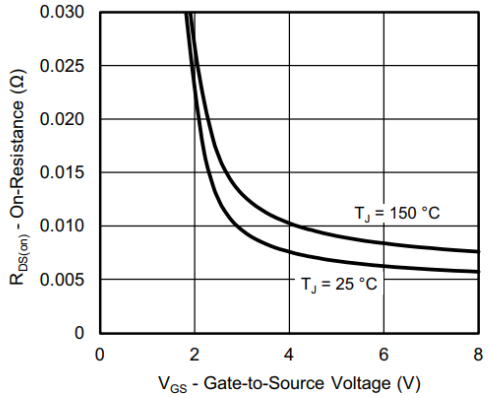

**Output Characteristics**



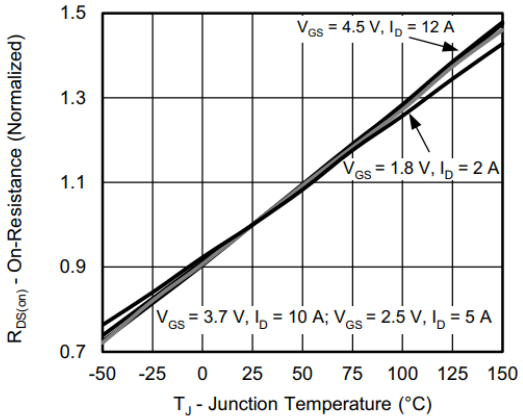

**Transfer Characteristics**



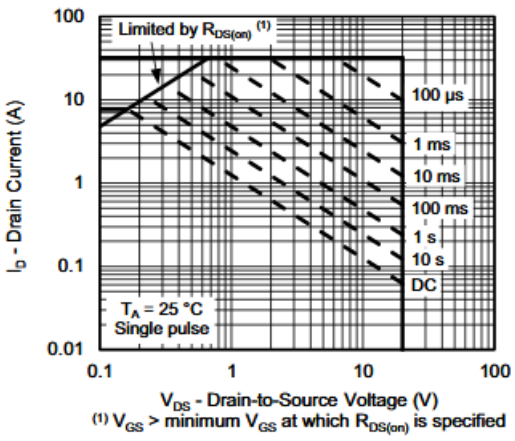

**On-Resistance vs. Drain Current and Gate Voltage**



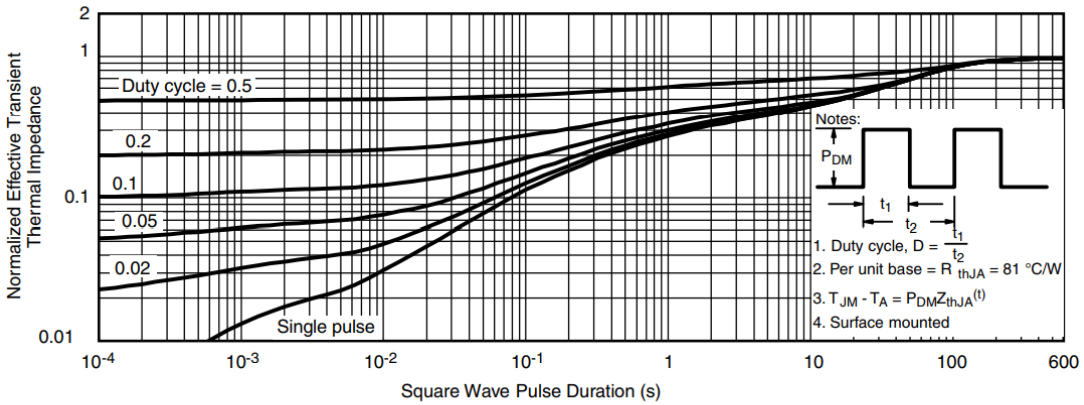

**On-Resistance vs. Gate-to-Source Voltage**




**On-Resistance vs. Junction Temperature**

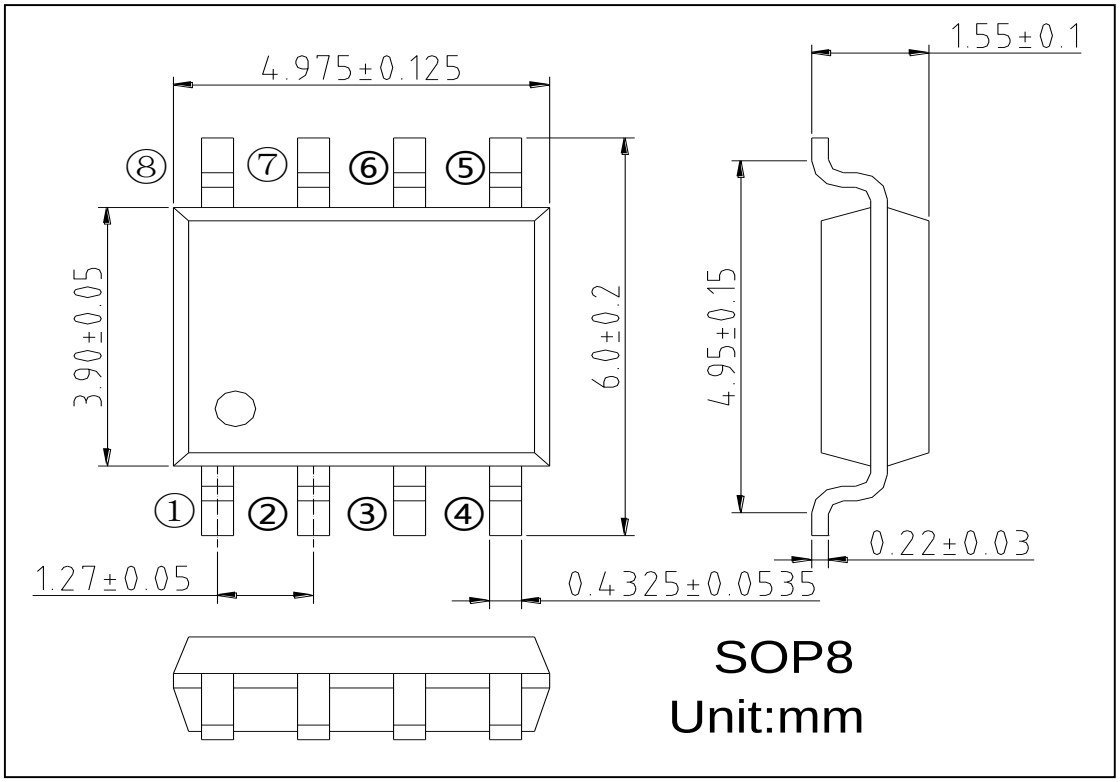



**Safe Operating Area, Junction-to-Ambient**




**Normalized Thermal Transient Impedance, Junction-to-Ambient**

## ➢ Package Information

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